IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: **DeWitt, Jr. et al.**	§	
	§	Group Art Unit: **2183**
Serial No. **10/675,778**	§	
	§	Examiner: **Johnson, Brian P.**
Filed: **September 30, 2003**	§	
	§	
For: **Method and Apparatus for Counting Data Accesses and Instruction Executions that Exceed a Threshold**	§	

Commissioner for Patents
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35525
PATENT TRADEMARK OFFICE
CUSTOMER NUMBER

REPLY BRIEF (37 C.F.R. 41.41)

This Reply Brief is submitted in response to the Examiner's Answer mailed on December 27, 2006.

No fees are believed to be required to file a Reply Brief. If any fees are required, I authorize the Commissioner to charge those fees which may be required to IBM Corporation Deposit Account No. 09-0447.

RESPONSE TO EXAMINER'S ANSWER

In the Appeal Brief filed September 29, 2006, Appellants asserted that Davidson does not anticipate claim 1 pursuant to the requirements of 35 U.S.C. § 102(b) in part because Davidson fails to disclose or suggest "responsive to receiving an instruction at a processor in the data processing system, determining whether an indicator is associated with the instruction, wherein a threshold value is located in the indicator" as recited in claim 1. Specifically, Appellants pointed out that Davidson fails to disclose or suggest either "wherein a threshold value is located in the indicator" or determining whether an indicator that has a threshold value located in the indicator is associated with an instruction "responsive to receiving an instruction at a processor in the data processing system."

Initially, with respect to the claim limitation "wherein a threshold value is located in the indicator", Appellants pointed out in the Appeal Brief that threshold values in Davidson are stored in threshold registers 521-525 illustrated in Figure 5B of the reference, and are not "located in the indicator" associated with an instruction as recited in claim 1.

In an effort to read claim 1 on the disclosure in Davidson, however, the Examiner contends that the instruction tag described in Col. 7, line 64 to Col. 8, line 32 of Davidson and the threshold value registers 521-525 illustrated in Fig. 5B and described in Col. 8, line 59 to Col. 9, line 2 of Davidson can collectively be construed as comprising the "indicator" recited in the claim; and, therefore, the Examiner concludes that the threshold value in Davidson is located in an indicator as required by claim 1.

In responding to Appellants' arguments in the Appeal Brief, the Examiner states:

> Applicant's invention and the teachings of Davidson both disclose an indicator (as being interpreted by the Office Action) as a short series of bits. Additionally, the fact that Davidson gives the names "threshold register" and "instruction tag" does not change the fact that these bits complete the same functionality as claimed by Applicant. Applicant's Specification on page 27 clearly describes indicators being used in the same way as Davidson's instruction tag and threshold registers; "[a] single bit may be used to indicate that events are to be counted in response to execution of that instruction"; [m]ultiple bits may be used to identify a threshold."

Examiner's Answer dated December 27, 2006, page 13.

Appellants respectfully disagree that Davidson's instruction tag and threshold registers are used in the same way as the indicator recited in claim 1. In Davidson, when an instruction is fetched, it may be selected and marked, and as a marked instruction flows through a pipeline unit, the pipeline unit signals its completion of the processing for the marked instruction by asserting a stage completion signal (see col. 7, line 64 to Col. 8, line 5 of Davidson). The instruction is thus marked only to indicate that it is to be monitored for completion of each stage of the instruction pipeline. The marking of the instruction has nothing to do with a threshold value, and a threshold value is not located in the marking disclosed in Davidson.

Threshold registers 521-525 in Davidson, on the other hand, store threshold values for each instruction pipeline stage of the instruction pipeline through which an instruction flows. These threshold values are associated with the instruction pipeline stages and not with the instruction. Any marked instruction that flows through the pipeline stages will be monitored based on the same threshold values specified in the threshold registers. These threshold values are thus unrelated to and are separate from the marking that indicates that an instruction is to be monitored (i.e., an indicator associated with the instruction), and is not located in the indicator. Therefore, Davidson does not disclose "wherein a threshold value is located in the indicator" as recited in claim 1. Davidson, in fact, actually teaches away from the present invention by teaching that threshold values are located in threshold registers that are associated with pipeline stages and that are separate from any indicator associated with an instruction.

In addition, with respect to the claim limitation "responsive to receiving an instruction at a processor in the data processing system, determining whether an indicator is associated with the instruction", Appellants pointed out in the Appeal Brief that Davidson does not determine whether an indicator in which a threshold value is located is associated with an instruction "responsive to receiving an instruction at a processor in the data processing system" as is recited in claim 1.

In responding to Appellants' arguments in the Appeal Brief, the Examiner states that the term "determining" means "to come to a decision or resolution", and asserts that "Davidson is required to determine (come to the resolution that) an indicator is associated with an instruction in response to receiving the instruction" (Examiner's Answer at page 15).

Appellants respectfully disagree. In Col. 7, lines 64-65, Davidson states "As an instruction is fetched, a single instruction may be selected and marked (or tagged)". If an instruction is marked, a stage completion signal will be asserted as the instruction flows through each pipeline unit of the instruction pipeline. Thereafter, thresholder 520 in Davidson compares the time intervals of each pipeline instruction stage with threshold values stored in the threshold registers 521-525 (see Col. 8, lines 59-62). Any determination that might be performed in Davidson, accordingly, relates to whether a stage completion signal should be asserted when an instruction flows through a pipeline unit, and is unrelated to determining whether an indicator in which a threshold value is located is associated with an instruction "responsive to receiving the instruction at a processor in the data processing system" as recited in claim 1. Therefore, Davidson also does not disclose or suggest determining whether an indicator in which a threshold value is located is associated with an instruction "responsive to receiving an instruction at a processor in the data processing system" as recited in claim 1.

For the above reasons and for the reasons set forth in the Appeal Brief, Davidson simply does not disclose or suggest "responsive to receiving an instruction at a processor in the data processing system, determining whether an indicator is associated with the instruction, wherein a threshold value is located in the indicator" as recited in claim 1, and does not anticipate claim 1; and it is respectfully requested that the Board reverse the Examiner's Final Rejection of that claim.

As indicated in the Appeal Brief, independent claims 9, 10, 11, 16, 19, 21 and 23-25 are also not anticipated by Davidson for similar reasons as discussed with respect to claim 1; claims 2, 4-8, 12-15, 17-18, 20 and 22 depend from and further restrict one of the independent claims and are also not anticipated by Davidson, at least by virtue of their dependency; and claim 3 depends from claim 1 and is not unpatentable over Davidson. It is, accordingly, respectfully requested that the Board also reverse the Examiner's Final Rejection of claims 1-25.

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